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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/160,824	09/25/1998	TSIU CHAN	97-C-108	6763

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EXAMINER

DICKEY, THOMAS L

ART UNIT PAPER NUMBER

2826

DATE MAILED: 05/03/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/160,824	CHAN ET AL.	
	Examiner	Art Unit	
	Thomas L Dickey	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 12 February 2002.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) 20 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-19 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- | | |
|----------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ | 6) <input type="checkbox"/> Other: |

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DETAILED ACTION

1. The amendment filed on 02/14/01 has been entered.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 7 and 9 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The limitation "contact pads on the active surface of the first integrated circuit chip for external connection to the central processing unit," which appears in both claims, is not supported by the original disclosure.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

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(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 1,3,4,6,8,10,11,13,14,16, and 18 are rejected under 35 U.S.C. 102(a) as being anticipated by Ma et al. (5,677,567).

Ma et al. discloses a chip assembly comprising a first integrated circuit chip 702 having an active face including a central processing unit; and a second integrated circuit chip 704 mounted on, and electrically connected to, the active face of the first integrated circuit, and a third integrated circuit chip 706 adjacent the second integrated circuit chip 704 wherein the second integrated circuit chip 704 adds functionality, *in the form of memory*, to the central processing unit of the first integrated circuit 702, the third integrated circuit chip 706 adds further functionality to the integrated circuit microprocessor, and the electrical connection between the first integrated circuit chip 702 and the second integrated circuit chip 704 is by using a bonding layer 708 to provide a direct connection of metal regions (712, 722, 726, and 732) that are integral with the active faces of the first 702 and second 704 chips, and where an active face of the second integrated circuit chip faces the active face of the first integrated circuit chip, the bonding layer 708 between and electrically connecting the metal regions (712,722,726, and 732) projecting from the active faces of the first and second integrated circuit chips, and metal region 712 projecting from the active face of the first integrated circuit chip 702 overlies metal region 726 projecting from a surface of the second integrated circuit chip 704, and where the metal re-

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gions (712, 722, 726, and 732) comprise conductive regions projecting from the active faces of the first and second chips and the active regions of the first and second chips are spaced apart by the metal regions. Note figure 7 and lines 40-67 of Ma et al. Note also that neither the instant claims nor the specification define the "bonding layer" (Ma et al's part 708, referred to by Ma et al. as a "lead frame") as anything more than a separate conductive layer between the chips which facilitates their bonding.

Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

A. Claims 2,5,15, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ma et al. (5,677,567).

Ma et al. discloses a chip assembly with all the limitations of these claims except that the central processing unit comprise either a digital signal processor or a field programmable gate array, the memory comprise one of cache, DRAM, SRAM, FLASH, or that the second integrated circuit chip comprise an analog-to-digital converter. Note figure 7 and lines 40-67 of Ma et al. However, DSP and SPGA are well

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known circuits for a CPU chip, likewise cache, DRAM, SRAM, and FLASH are well known types of memory chips, and A-D converters are commonly put in small, auxiliary chips such as the second integrated circuit chip. Therefore, it would have been obvious to a person having skill in the art to replace the circuits of Ma et al.'s chip assembly with the circuits such as DSP, SPGA, cache, DRAM, SRAM, FLASH, and A-D converters in order provide a practical use for Ma et al.'s chip assembly.

B. Claims 12 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ma et al. (5,677,567) in view of Raad (5,869,895).

Ma et al. discloses a chip assembly with all the limitations of these claims except that a width of the second integrated circuit chip is less than a width of the first integrated circuit chip, and a length and width of the second integrated circuit chip are less than a respective length and width of the first integrated circuit chip. However, Raad discloses a memory array stacked on a CPU chip with second integrated circuit chips 103 over a first integrated circuit chip 101 where the length and breadth (i.e., width) of the second integrated circuit chips 103 is both less than the length and breadth of the first integrated circuit chip. Note figure 1 of Raad.

Therefore, it would have been obvious to a person having skill in the art to replace the generally disclosed second integrated circuit chip of Ma et al.'s chip assembly with the second integrated circuit chip having a smaller "profile" such as

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taught by Raad in order to have the capacity to place more than one second integrated circuit chip on a first integrated circuit chip to thus provide better flexibility in circuit design, especially the ability to place multiple memory chips on a single CPU.

Response to Arguments

5. Applicant's arguments filed 02/16/00 have been fully considered but they are not persuasive.

It is argued, at page 10 of the remarks, that "[Ma et al. does not describe a device that anticipates claims 1,4,10-11,13,16, and 18, because] Independent claims 1 and 13 each recite that the second chip is mounted on the active face of the first chip, [and] Ma et al does not teach ... mounting one integrated circuit directly on the active surface of another." However, it is noted that the feature upon which applicant relies (i.e., mounting directly on) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

At page 12 of the remarks, it is further argued, that "[Ma et al., alone or combined with Raad, does not suggest the subject matter of claims 2,3,5-9,12,14,15,17, or 19, because] As noted above, independent claims 1 and 13 each recite mounting the second chip directly on the active face of the first chip." However, "the word "directly"

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appears in applicants' arguments but not in their claims. "Directly on" has a meaning distinct from "on," and in light of the discussion of "bonding layers" in the specification "on" cannot, in this case, be considered to have been used, by applicants to mean "directly on," in claims 1 and 13. Note further that applicants cannot reasonably argue that "on" means "directly on" in claim 13, when claim 14 further limits claim 13 by "the active regions of the first and second chips [being] spaced apart by the metal regions."

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing

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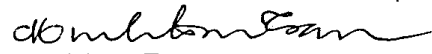
date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 703-308-0980. The examiner can normally be reached on Monday through Thursday 8 AM to 6 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703) 308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 306-3431.

tld
04/2002


Minh Loan Tran
Primary Examiner